Challenges and Improvement of Reliability in Advanced Wafer Level Packaging Technology

by

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***Abstract*- The number of WLCSP (Wafer Level Packages) used in semiconductor packaging has experienced significant growth since its introduction in 1998. The growth has been driven primarily by mobile consumer products because of the small form factor and high performance enabled in the package design. And it is also attractive to WE (wearable electronics) and IoT (Internet of Things) products. Although WLCSP is now a widely accepted package option, the initial acceptance of WLCSP was limited by concerns with the SMT assembly process and the fragile nature of the exposed silicon inherent in the package design. Assembly skills and methods have improved since the introduction of the package; however, damage to the silicon remains a concern. The side or top of the die continue to be exposed after dicing the wafer and the silicon continues to be at risk for chipping, cracking, and other handling damage during the assembly process.**

This paper introduces eWLB (embedded Wafer Level Ball Grid Array) /FO-WLP (fanout–WLP) and eWLCSP (encapsulated WLCSP) for its improved and advanced reliability [1]. In these new packages EMC is applied to all exposed silicon surfaces on the die. The manufacturing process leverages existing high volume manufacturing methods with exceptionally high process yields. eWLB is a type of FO-WLP that has the potential to realize any number of interconnects with standard pitches at any shrink stage of the wafer node technology. For eWLCSP, the applied coating protects the silicon and fragile dielectrics to prevent handling damage during dicing and assembly operations, effectively providing a packaged part in the form factor of a WLCSP. In manufacturing process, the product wafer is thinned and diced first. The dies are then reconstituted into a wafer form and standard methods are used to apply dielectrics, thin film metals, and solder bumps. The resulting structure is identical to conventional WLCSP products with the exception of the protective sidewall coating.

This paper discusses the improvement of reliability, both component level and board level (drop and Temperature Cycle on Board). The key attributes of the new package as well as the manufacturing process used to create it are to be presented. Experimental reliability data and failure mode are studied and compared to conventional WLCSP products.

I. Introduction

The wafer level chip scale package (WLCSP) was introduced in the late 1990's as a semiconductor package wherein all manufacturing operations were done in wafer form with dielectrics, thin film metals and solder bumps directly on the surface of the die with no additional packaging [2]. The basic structure of the WLCSP has an active surface with polymer coatings and bumps with bare silicon (Si) exposed on the remaining sides and back of the die. The WLCSP is the smallest possible package size since the final package is no larger than the required circuit area. The number of WLCSP used in semiconductor packaging has experienced significant growth since its introduction due to the small form factor and high performance requirements of mobile consumer products.

Although WLCSP is now a widely accepted package option, the initial acceptance was limited due to concerns with the Surface Mount Technology (SMT) assembly process and the fragile nature of the exposed silicon inherent in the package design. Assembly skills and methods have improved since the introduction of WLCSP; however, damage to the exposed silicon remains a concern. This is particularly true for advanced node products with fragile dielectric layers. One method commonly used to improve die strength and reduce silicon chipping during assembly is lamination of an epoxy film on the back of the die (BSC, backside coating) as shown in Fig.2. By the nature of the backside lamination process, the uncoated sides of the die continue to be exposed after dicing the wafer and the silicon continues to be at risk for chipping, cracking and other handling damage during the assembly process.

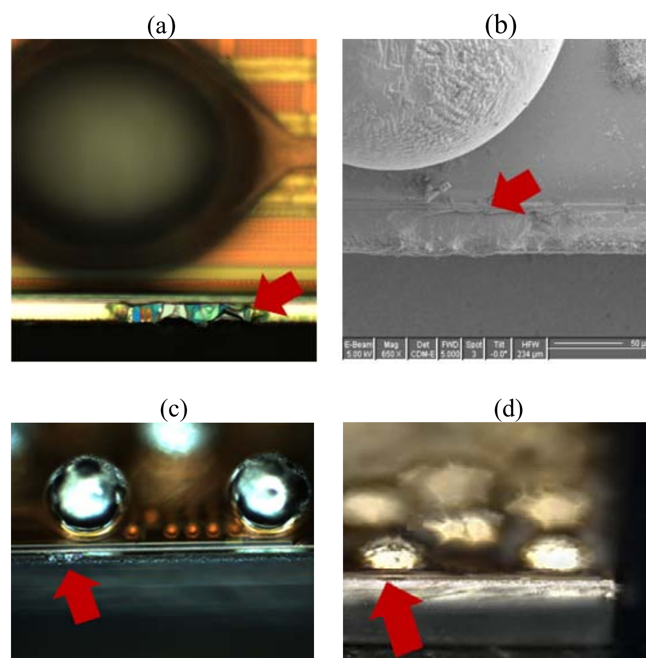


Figure 1. Defects of WLCSP (a-c) side wall chipping after singulation and (d) defect found after SMT process

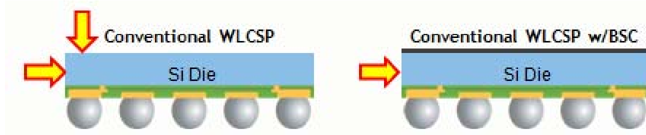


Figure 2. Potential defect areas (chipping or mechanical damage) of (a) WLCSP and (b)WLCSP with Backside coating

A new process has been developed to provide five-sided protection for the exposed silicon in a WLCSP. The ability to apply a protective coating to all the exposed die surfaces in a WLCSP is based on an existing high volume manufacturing flow developed for fan-out products known as embedded Wafer Level Ball Grid Array (eWLB). Unlike conventional WLP, the first step in eWLB manufacturing is to thin and singulate the incoming silicon wafer. Although this is commonly done for other semiconductor package formats, it has not been practiced for conventional WLCSP.

II. Innovative WLCSP with Sidewall Protection

A protective coating can be cost effectively applied to the exposed Si surfaces in a WLCSP, thereby addressing the chipping, cracking and other handling damage that can occur during the assembly process. The new WLCSP follows the same process flow as eWLB [3]. Reconstituted wafers are processed with conventional wafer level packaging techniques for the application and patterning of dielectric layers, thin film metals for redistribution and under bump metal and solder bumps. In the final dicing operation a thin layer of molding compound, typically 30µm, is left on the side of the die as a protective layer. The back of the die is also protected with molding compound, although with a greater thickness. The result is a new encapsulated WLCSP (eWLCSP) which has an increased level of durability and reliability over traditional WLCSP designs.

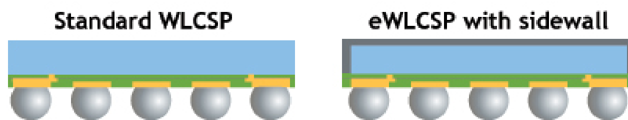


Figure 3. eWLCSP Structure of WLCSP and eWLCSP

The significant benefit of encapsulation is the light and mechanical protection for the bare die. The eWLCSP structure is equivalent to conventional WLCSP with the addition of a thin protective coating on the four sidewalls of the die. A schematic drawing of a typical structure is shown in Figure 4 for greater clarity. Alternatively, the backside molding compound can be removed and the body made thinner with an optional back grind operation without damaging the protective sidewall layer. The remaining sidewall coating will continue to protect the fragile silicon sides of the die during the assembly operation. Figure 5 shows the micrographs of eWLCSP with SEM and optical view.

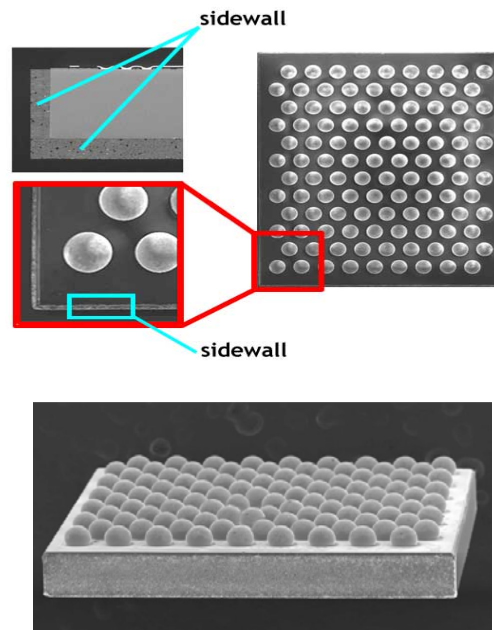


Figure 4. Micrographs of eWLCSP

III. Structure of the Encapsulated WLCSP

In FO WLP, the area of the package is increased to allow for placement of redistribution layers (RDL) and solder balls outside of the silicon die area. This allows the die to shrink to a minimum size independent of the required area for an array of solder balls at industry standard BGA ball pitches [4]. It also enables novel multi-die structures, 2.5D structures and 3D structures. In the case of conventional FO WLP, die are typically widely spaced to allow for the expanded RDL and bump area and the conventional saw street. In the case of eWLCSP, the dies are closely spaced, allowing for only the sidewall thickness in addition to a saw street area. The eWLCSP process data presented here was generated with a 300mm round reconstituted panel [4]. The final structure had 2 layers of polymer and 1 layer of plated Cu RDL with the solder ball mounted directly on the RDL without the use of a separate UBM layer.

IV. Advantages of the Encapsulated WLCSP [4]

eWLCSP would seem to have a higher cost over conventional WLCSP since there are additional steps required for reconstitution at the start of the FlexLine™ manufacturing flow. There are key factors, however, that offset the cost of the additional steps required for the reconstitution to make this a commercially viable process.

(1) Cost-effectiveness:

eWLCSP is fabricated using reconstitution. Good die from the parent wafer are picked and transferred to a (larger) reconstituted carrier. Since the majority of WLCSP products use 200mm wafers, reconstitution enables the scaling of the manufacturing process from the 200mm wafer to the size of the

carrier in eWLB technology. This carrier size ranges from 200/300mm to a larger format like high density (HD) with ~ 20% greater area or ultra high density (UHD) with > 300% greater area. The scaling of the manufacturing process with reconstitution far outweighs the cost of reconstitution itself, thereby enabling large net cost reductions. Additionally, the ability to selectively pick good die from the parent wafer presents an additional net cost benefit as most wafers have a less than 100% wafer sort yield. Last but not least, the ability to pool the volume of traditional eWLB packages seamlessly together with eWLCSP packages on the same FlexLine^{TM} provides important economies of scale. With the three factors stated above, significant net cost reductions over traditional WLCSP front end processing are achievable, depending on the original wafer diameter, the carrier format used for reconstitution (300mm, HD or UHD) and the yield of incoming wafers.

(2) High Quality Solutions:

The polymer sidewall structure of eWLCSP all but eliminates mechanical damage such as chipping and cracking that is commonly encountered in traditional WLCSP processing. This serves to eliminate many expensive steps such as back side coating or lamination and complex inspection steps that are currently necessary for standard WLCSP to manage mechanical damage and ensure product quality. More fundamentally, the eWLCSP allows customers to *build in quality by design* vs. using inspection to weed out defects. This has implications for reducing the risk of field failure due to the shipment of marginally defective parts that may escape inspection. As is shown in a later section, the encapsulated eWLCSP structure has also helped to increase the overall die strength by ~ 100% in addition to the mitigation of cracking and chipping defects, making for an overall more robust package.

(3) Investment and Infrastructure – Wafer Agnostic Processing:
In traditional WLCSP processing, the investment and infrastructure for manufacturing are based on the diameter of the incoming wafer. This creates a financial burden to re-tool the manufacturing lines to provide the needed capacity (to meet market demand) as wafer transitions occur (e.g. from 200 mm to 300 mm or from 300 mm to 450 mm in future) while also having to obsolete the existing manufacturing assets. The FlexLine^{TM} approach for eWLB and eWLCSP effectively decouples the packaging process from the incoming wafer altogether obviating the above-described financial burden resulting from wafer diameter transitions.

(4) Design Friendly – Allows seamless transition from fan-in to fan-out within the same basic package platform:

As noted previously, the standard fan-in WLCSP only works below a certain threshold of I/O density, based on the minimum allowable terminal I/O pitch. The threshold is ~ 4 I/O /mm2 for a 0.5 mm terminal I/O pitch and ~ 6 I/O /mm2 for 0.4 mm terminal I/O pitch. Small changes in I/O density that commonly occur with changes in Si design, die shrinks resulting from Si node transitions may lead to a given design exceeding the WLCSP threshold, causing the design to "fall off" the WLCSP application space envelope, necessitating a change in packaging POR to traditional substrate- or leadframe-based packages like FBGA, fcBGA, QFN etc. These packages are fundamentally different than WLCSP in terms of footprint, form factor, performance and cost, resulting in a major "reset" in the packaging POR. In contrast, the eWLCSP may be viewed as part of the more universal eWLB platform wherein the aforementioned I/O density transitions can be seamlessly accommodated within the same packaging platform. For designs whose I/O density falls marginally outside the threshold, an additional row of terminal solder balls can be added without fundamentally altering the package structure, form factor or performance.

V. Reliability of Larger eWLCSP over 6×6 mm Package Size

Robust reliability of 4.5x4.5mm eWLCSP was reported with Component Level Reliability (CLR) and Board Level Reliability (BLR) tests [3]. For reliability tests of larger eWLCSP over 6x6mm, two test vehicles were prepared, 6x6mm and 8x8mm as shown in Table 2. The eWLCSP process passed standard reliability tests used in wafer level packaging including CLR and BLR (TCoB and drop test). CLR was completed with the test conditions shown in Table 3 [5].

Table 1. eWLCSP Test Vehicle Details

	eWLCSP size	Mask No.	Solder ball pitch
TV1	6x6mm	3 (without UBM)	0.4mm
TV2	8x8mm	4 (with UBM)	0.35mm

The evaluation results were confirmed by visual inspection and electrical test. No delamination of the protective coating was detected during the CLR evaluation. TCoB was completed and passed 500 cycles with the results shown in Table 4. Results obtained from electrical measurement of daisy chain bump structures demonstrate eWLCSP is comparable to conventional WLCSP product produced with polyimide dielectrics. Drop test was completed and passed the JEDEC requirement with the results shown in Table 4.

The 4-point bending test was carried out to investigate package level strength. eWLCSP shows over 25% increase in die strength compared to WLCSP due to the sidewall protection and optimized backgrinding process. The Si surface roughness also was measured with atomic force microscopy (AFM). eWLCSP has quite a close Si roughness value to WLCSP. A roughness image scan clearly showed no difference in Si surface roughness between WLCSP and eWLCSP.

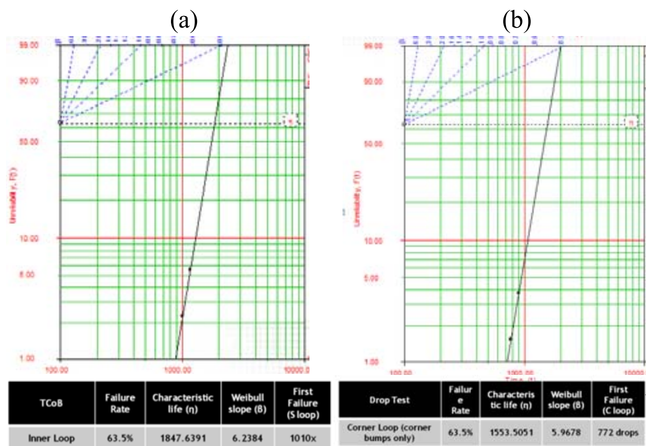
The protective sidewall coating is a unique attribute of the eWLCSP package. This protective layer is durable and will prevent silicon chipping on the side of the package and has the ability to protect the silicon during socket insertion for test. This has been demonstrated through multiple insertion tests on completed products with no observed damage to the protective coating in Table 4 and 5.

Table 2. Component Level Reliability Results

Component Level Test	Condition		Status
MSL1	MSL1, 260ºC Reflow (3x)	-	Pass
Temperature Cycling (TC) after Precon	-55ºC to 125ºC	1000 x	Pass
HAST (w/o bias) after Precon	130ºC / 85% RH	192 hrs	Pass
High Temperature Storage (HTS)	150ºC	1000 hrs	Pass

Table 3. Board Level Reliability Test Results

Tests	Conditions	Status
TCoB	JEDEC JESD22-A103 -40ºC to 125ºC	Pass
Drop Test	JEDEC JESD22-B111 1500G	Pass



TCoB	Failure Rate	Characteristic life (η)	Weibull slope (β)	First Failure (S loop)
Inner Loop	63.5%	1847.6391	6.2384	1010x

Drop Test	Failure Rate	Characteristic life (η)	Weibull slope (β)	First Failure (C loop)
Corner Loop (corner bumps only)	63.5%	1553.5051	5.9678	772 drops

Figure 5. Weibull plots of (a) TCoB and (b) drop test result.

Table 4. VM scan yield summary after Auto-handler Socket Insertion Test

VMScan Yield Summary Results	Pre VMScan	lx Socket Insertion PostVMScan	2x Socket Insertion PostVMScan	3x Socket Insertion PostVMScan
#of Devices Inspected SOU	5000	5000	5000	5000
#of Devices Accepted	5000	5000	5000	5000
VMYield	100.00%	100.00%	100.00%	100.00%
# of Devices Rejected	0	0	0	0

Table 5. Visual inspection result after multiple Auto-handler Socket Insertion Test (Passed Sample No. /Tested Sample No.)

Pre-Visual Inspection	**Post Visual Inspection (1x socket insertion)**	**Post Visual Inspection (2x socket insertion)**	**Post Visual Inspection (3x socket insertion)**
249/249 (100% Yield)	249/249 (100% Yield)	249/249 (100% Yield)	249/249 (100% Yield)

With these test results along with component and board level reliability results, eWLCSP with additional sidewall protection has demonstrated more robust reliability than standard WLCSP and prevents side chip cracking.

VI. CONCLUSIONS

Growing demand for WLCSP in a range of advanced mobile products is driving the need to cost effectively reduce risk of cracking, chipping and handling issues before or during the SMT assembly process. As mobile device manufacturers tighten their technical specifications to reach new levels of reliability in their products, the industry will see more stringent component level and board level reliability (BLR) requirements. eWLCSP is a robust packaging solution that cost effectively addresses the increased durability requirements for our customers in advanced silicon nodes down to 28nm.

A new encapsulated WLCSP process has been developed and verified with reliability testing. The process provides mechanical sidewall protection to WLCSP parts with thin polymer coating. The mechanical sidewall protection that is now possible in eWLCSP devices resolves the problem of silicon damage during the assembly process and provides a path to significant cost savings for customers as the manufacturing panel size is increased. eWLCSP passed JEDEC component and board level reliability even for larger body size of 8x8mm.

The eWLCSP process is also wafer size agnostic, so the same manufacturing line can process the eWLCSP products regardless of the incoming wafers size. As mobile device manufacturers tighten their technical specifications to reach new levels of reliability in their products, the industry will see more stringent component level and board level reliability (BLR) requirements. eWLCSP is a robust packaging solution that cost effectively addresses the increased durability requirements for our customers in advanced silicon nodes down to 28nm."

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