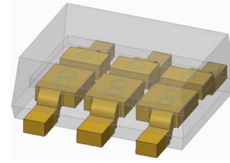
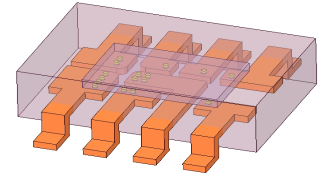
FCOL

Flip Chip On Leadframe

JCET offers Flip Chip on Leadframe (FCOL) in both SOT and TSOT package configurations. FCOL provides a cost effective option for chip scale packaging for devices with low IO counts from 3 - 8L. JCET offers a full turnkey solution for FCOL from wafer bumping and assembly to final test.





Highlights

- High density SOT & TSOT leadframes
- TSOT FCOL supports multiple lead counts: 3, 5, 6, 8L
- Wafer bumping available at two JCET factories

Features

- FCOL package outline sizes of 1.63 x 1.60 x 0.58mm and 2.9 x 2.8 x 0.9mm
- Minimum flip chip bump diameter of 100um
- 15um RDL thickness on bumped die
- Minimum of 150um bumped die thickness
- High thermal solution with high thermal compound

Standard Materials

- Die Bump 1P1M/2P2M+Solder Ball
- Leadframe Copper + OSP
- Compound 45un maximum filler size
- I/O finish Sn plating

Applications

- PMIC
- AC-DC / DC-DC
- LNA
- RF Switch
- PA
- Power
- Audio

Process Highlights

- Package thickness 0.58mm-0.90mm
- Die thickness 150um minimum
- Die to package edge 150um minimum
- Bump height 100um/80um/70um
- Bump to lead edge 30um minimum
- Bump to hole 50um minimum
- Hole to package edge 125um minimum

Package Level Reliability

- Moisture Sensitivity Level JEDEC Level 1 @ 260 C
- Temperature Cycling –65°C to 150°C, Dwell: 15 min
- Pressure Cooker Test 121°C/100%RH 205 Kpa
- THT 85°C/85% RH
- HTST Ta = 150C

Thermal Performance

Typical thermal resistance is <10C/W, significantly lower than the traditional package which is typically 10-20C/W.

Electrical Performance

- High current applications
- Low RDSON performance
- Dependent on application design

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