PoP

Package-on-Package: VFBGA-PoPb-SDx, L/TFBGA-PoPt-SDx

Highlights

- Stacking fully tested memory & logic packages eliminates known good die (KGD) issues
- Package-on-package stacking provides flexibility in mixing and matching IC technologies
- Devices can be procured from multiple manufacturing sources
- Meets accepted package & board level reliability standards for CSP

Features

- CuOSP or Ni/Au on bottom pads of bottom PoP (PoPb) with lead free ball options
- Ni/Au on top memory interface pads of PoPb
- 0.4mm min. ball pitch on bottom / BGA pads & 0.65mm pitch on top memory interface pads of PoPb
- CuOSP or Ni/Au on bottom pad of top PoP (PoPt) with lead free ball options
- Top pin gate molding for PoPb (top center gate mold)
- Low stress and warpage die attach adhesives
- Low stress and warpage mold compound
- PoPb height less than 0.9mm (VFBGA-PoPb)
- PoPt height less than 1.0mm for 3 die stack (VFBGA-PoPt-SD3)
- PoPt height less than 1.2mm for 4 to 5 die stack (TFBGA-PoPt-SD5)
- Total package height dependent on PoPt configuration, but min. 1.4mm possible
- Full in-house electrical, thermal and mechanical simulation and measurement capability
- Full in-house package and substrate design capability

Applications

- PoPb: Cellular phone digital baseband processor, digital die stack, or digital + analog baseband die stack
- PoPt: Cellular phone memory for digital processor and system memory (SDRAM, NOR/NAND Flash, SRAM)

Test Services

- Product Engineering support
- Probe capability
- Program generation/conversion
- Drop ship available

TFBGA-PoPt-SD3
VFBGA-PoPb
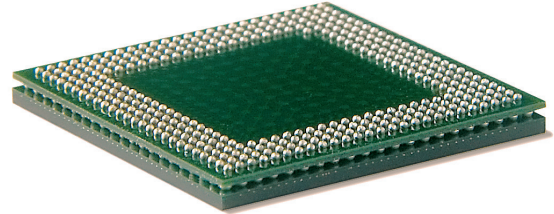
Description

Our Package-on-Package (PoP) family includes a stackable FBGA as the bottom PoP package (PoPb). PoPb is typically an ASIC or baseband device with land pads placed on the top periphery of the package surface to enable the stacking of a second FBGA or PoP top (PoPt) above. PoPt consists of memory or other silicon functionally assembled, tested and yielded independently. The two packages are combined by reflowing together (usually performed simultaneously) on the application board, to form PoP (Z-interconnection with solder ball). We offer the flexibility of stacking up to two devices in the PoPb and up to five devices in the PoPt.

Advantages

As multi-die stacking becomes increasingly more common, known good die issues are critical for cost saving and throughput yield. For example, in a four die stack package, a single die can render the entire package unusable even if the other three die are fully functional. One way to overcome this problem is by using package stacking which can overcome known good die issues since die functionality can be checked after being packaged and before being placed on top of another known good package.

PoP can provide an overall low profile as stacked and allows individual packages to be tested prior to stacking. This PoP approach is attractive to device manufacturers and end customers. Device manufacturers can focus on their core competencies and not worry about integrating other devices (test and yield implications) into the packages they sell. The end customer can leverage traditional sources for each device type and has more flexibility to configure devices as needed for a particular product and market.

Specifications

Die Thickness	60-100mm range performed (2.5-4.0mils)
Gold Wire	18-25µm (0.7 - 1.0mils) diameter
Solder Balls	Sn/Ag/Cu (Pb-free) ball
Marking	Laser
Packing Options	JEDEC tray or tape & reel

Reliability

Moisture Sensitivity Level	JEDEC Level 2A (260°C IR)
Temperature Cycling	TC-C, –65°C to 150°C, 1000 cycles
Temperature/Humidity Test	85°C/85%, RH, 1000 hrs
Highly Accelerated Stress Test	135°C/85%, 100% RH, 96 hrs
High Temperature Storage	150°C, 1000 cycles

Thermal Performance θja (°C/W)

Thermal performance is highly dependent on the location of power dissipation, especially for the upper package devices. Detailed thermal modeling is used to accurately determine the actual thermal behavior of each specific PoP project.

Package	Body Size (mm)	Position	Pincount	Die Size (mm)	Power (W)	T-junction (C)*	Thermal Performance θja (C/W)
VFBGA-PoPb	14 x 14	Lower	352	8.4 x 8.0	0.6	116.7	17.6
TFBGA-PoPt-SD2	14 x 14	Upper	152	8.0 x 8.0 (PoPt - bottom die)	0.6	127	23.3
				8.0 x 6.0 (PoPt - top die)	0.6	129.1	24.5

Notes: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2. *T-ambient = 85°C. **θja is based on total power dissipation.

Electrical Performance

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

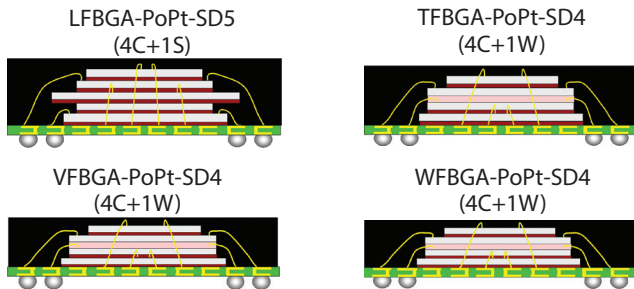| Conductor Component	Length (mm)	Resistance (mOhms)	Inductance Self (nH)	Inductance Mutual (nH)	Capacitance Self (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	34 - 119	1.3 - 4.55	0.26 - 2.28	0.25 - 0.95	0.06 - 0.42
Total (2L)	4 - 9	154 - 239	2.95 - 6.20	0.71 - 3.13	0.35 - 1.05	0.07 - 0.44
Net (4L)	2 - 7	34 - 119	0.90 - 3.15	0.18 - 1.58	0.35 - 1.10	0.06 - 0.42
Total (4L)	4 - 9	154 - 239	2.55 - 4.80	0.63 - 2.43	0.45 - 1.20	0.07 - 0.44

Note: Results are simulated values per JEDEC EIA/JEP123 standards.
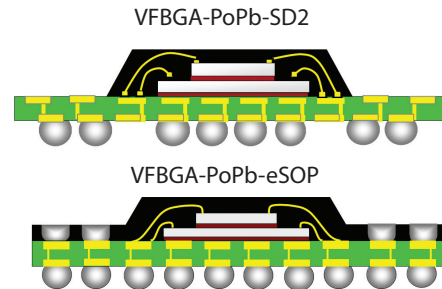
Package Configurations

Package	Body Size (mm)	Lead Count
VFBGA-PoPb-SDx	12 x 12, 14 x 14, 15 x 15	200 ~ 700
T/LFBGA-PoPt-SDx	12 x 12	128
	14 x 14	152
	15 x 15	160

Cross Section L=1.4mm, T=1.2mm, V=1.0mm, W=0.8mm

Top PoP (PoPt)

LFBGA-PoPt-SD5
(4C+1S)

TFBGA-PoPt-SD4
(4C+1W)

VFBGA-PoPt-SD4
(4C+1W)

WFBGA-PoPt-SD4
(4C+1W)

Bottom PoP (PoPb)

VFBGA-PoPb-SD2

VFBGA-PoPb-eSOP

Pre-Stacked PoP